

# Vita

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EDUCATION	<b>Ph.D. in Computer Science</b> Thesis: Techniques For Reducing The Computational Requirements Of Symbolic Reachability Analysis	University of Pennsylvania
	<b>M.S. in Computer Science</b> Thesis: Performance Analysis of Symbolic Reachability Algorithms in Model Checking	Rice University
	<b>B.S. in Computer Science</b>	University of Science and Technology of China
ACADEMIC AND PROFESSIONAL EMPLOYMENT	<b>Assistant Professor</b> , <i>Western Michigan University</i>	August 2003 - present
	<b>Consultant</b> , <i>NEC Labs America, Inc</i>	August 2003 - August 2005
	<b>Research Associate</b> , <i>NEC Labs America, Inc</i>	August 1999 - August 2003
	<b>Summer Visiting Scholar</b> , <i>EECS, University of Michigan</i>	May 1997 - August 1999
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RESEARCH GRANTS AND CONTRACTS	<ol style="list-style-type: none"><li>Trace-Driven Verification of Multithreaded Software. National Science Foundation. \$400,000. Lead Principal Investigator. (In collaboration with Karem Sakallah, EECS, University of Michigan). 09/01/2008-08/31/2011.</li><li>Continuously Monitoring and Checking Software in the Era of Multicore Systems. Office of Naval Research (ONR). PI: Liqiang Wang (University of Wyoming), Co-PI: Zijiang Yang. \$142,965. 4/10/2009-03/31/2011.</li><li>Integrated Testing and Analysis of Concurrent Programs. NEC Research Grant. Principal Investigator. \$20,000, 03/2008-12/2008.</li><li>Semantic Partial Order Reduction. NEC Research Grant. Principal Investigator. \$10,000, 09/2007-03/2008.</li><li>Guided Search For Software Verification. NEC Research Grant. Principal Investigator. \$20,000, 03/2007-12/2007.</li><li>Efficient Model checking C Program. NEC Research Grant. Principal Investigator. \$10,000, 09/2006-03/2007.</li><li>F-Soft Verification Platform. NEC Research Grant. Principal Investigator. \$20,000, 09/2005-09/2006.</li><li>An Advanced Itinerary Driven Mobile Agent System. Faculty Research and Creative Activities Support Fund. Principal Investigator. Western Michigan University. \$9550. 05/2006-05/2007.</li><li>Research Development Award. Western Michigan University. \$3500. 05/2005-12/2006</li></ol>	

### Journal Papers

1. Zijiang Yang, Chao Wang, Aarti Gupta, Franjo Ivancic, *Model Checking Sequential Software Programs Via Mixed Symbolic Analysis*, ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 14, Issue 1, January, 2009, ACM.
2. F.Ivancic, Z. Yang, M. Ganai, A. Gupta, and P.Ashar, *Efficient SAT-based Bounded Model Checking for Software Verification*, Theoretical Computer Science (TCS), Volume 404(3), September 2008, pages 256-274, Elsevier.
3. Z. Yang, S. Lu and P. Yang, *Trustworthy and Dynamic Mobile Task Scheduling in Data-Intensive Scientific Workflow Environments*, Journal of Autonomic and Trusted Computing. Accepted for Publication.
4. Z. Yang, S. Lu and P. Yang, *Model Checking Approach to Itinerary-based Access Control Enforcement of Mobile Tasks in Scientific Workflows*, Journal of Autonomic and Trusted Computing. Accepted for Publication.
5. Aleksandr Zaks, Zijiang Yang, Ilya Shlyakhter, Franjo Ivancic, Srihari Cadambi, Malay K. Ganai, Aarti Gupta, and Pranav Ashar, *Bitwidth Reduction via Symbolic Interval Analysis for Software Model Checking*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), volume 27(8), August 2008, IEEE.
6. Chao Wang, Franjo Ivancic, and Aarti Gupta, *Disjunctive Image Computation for Software Verification*, ACM Transactions on Design Automation of Electronic Systems, (TODAES), volume 12(2), April 2007, article 10, ACM. **ACM TODAES 2008 Best Paper Award.**
7. Malay Ganai, Aarti Gupta, Zijiang Yang and Pranav Ashar, *Efficient Distributed SAT and SAT-based Distributed Bounded Model Checking*, International Journal on Software Tools for Technology Transfer (STTT), Volume 8, Numbers 4-5, August 2006, Springer.

### Conference/Workshop Papers

1. Qichang Chen, Liqiang Wang, Zijiang Yang. *A Combined Static and Dynamic Approach for Escape Analysis*, To appear in the 33rd Annual IEEE International Computer Software and Applications Conference (COMPSAC) . Seattle, Washington. IEEE Press, 2009.
2. Qichang Chen, Liqiang Wang, Zijiang Yang, and Scott D. Stoller. *HAVE: Integrated Dynamic and Static Analysis for Atomicity Violations*, International Conference on Fundamental Approaches to Software Engineering (FASE), European Joint Conferences on Theory and Practice of Software (ETAPS). York, UK. Springer-Verlag, 2009.
3. Z. Yang, B. Al-Rawi, K. Sakallah, X. Huang, S.A. Smolka and R. Grosu. *Dynamic Path Reduction for Software Model Checking*, The 7th International Conference on Integrated Formal Methods, Duesseldorf, Germany, February 2009, Springer, LNCS.
4. Zijiang Yang and Karem Sakallah, *SMT-based Symbolic Model Checking for Multi-Threaded Programs*, position paper, Exploiting Concurrency Efficiently and Correctly (EC<sup>2</sup>), Princeton, NJ, July 2008.
5. C. Wang, Z. Yang, and A. Gupta, *Peephole Partial Order Reduction*, 14th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), Budapest, Hungary, April 2008.
6. Chao Wang, Zijiang Yang, Aarti Gupta, and Franjo Ivancic, *Using Counterexamples for Improving the Precision of Reachability Computation with Polyhedra*, 19th International Conference on Computer Aided Verification (CAV), Berlin, Germany, July 3-7, 2007.
7. Sa'ed Abed, Otmane A. Mohamed, Zijiang Yang, and Ghiath A. Sammane, *Integrating SAT with Multiway Decision Graphs for Efficient Model Checking*, The 19th IEEE international conference on Microelectronics, Cairo, Egypt, December 29-31, 2007.

8. Z.H. Kamal, A. Gupta, L. Lilien, and Z. Yang, *The MicroOppnet Tool for Collaboration Experiments with Class 2 Opportunistic Networks*, The 3rd International Conference on Collaborative Computing: Networking, Applications and Worksharing (CollaborateCom 2007), White Plains, New York, November 12-15, 2007.
9. P. Yang, Z. Yang, and S. Lu, *Formal Modeling and Analysis of Scientific Workflows Using Hierarchical State Machines*, 2nd International Workshop on Scientific Workflows and Business Workflow Standards in e-Science, held in conjunction with IEEE international conference on e-science and grid computing, 2007.
10. Zijiang Yang, Shiyong Lu and Ping Yang, *Itinerary-Based Access Control for Mobile Tasks in Scientific Workflows*, The 2007 IEEE International Symposium on UbiSafe Computing (UbiSafe), Niagara Falls, Ontario, Canada, May 21-23, 2007.
11. Leszek Lilien, Ajay Gupta, and Zijiang Yang, *Opportunistic Networks for Emergency Applications and Their Standard Implementation Framework*, The First International Workshop on Next Generation Networks for First Responders and Critical Infrastructure (NetCri07), New Orleans, Louisiana, April 11-13, 2007.
12. Chao Wang, Zijiang Yang, Aarti Gupta, and Franjo Ivancic, *Whodunit? Causal Analysis for Counterexamples*, Fourth international symposium on Automated Technology for Verification and Analysis (ATVA'06), Beijing, China, 2006.
13. Zijiang Yang, Chao Wang, Aarti Gupta, and Franjo Ivancic, *Mixed Symbolic Representations for Model Checking Software Programs*, ACM/IEEE International Conference on Formal Methods and Models for Codesign (Memocode'06), Napa, California, USA, 2006.
14. Zijiang Yang, Shiyong Lu, and Ping Yang, *Runtime Security Verification for Itinerary-Driven Mobile Code*, IEEE International Symposium on Dependable, Autonomic and Secure Computing (DASC'06), Indiana University, Purdue University, Indianapolis, USA, 2006.
15. Aleks Zaks, Ilya Shlyakhter, Franjo Ivancic, Zijiang Yang, Srihari Cadambi, Malay Ganai, Aarti Gupta and Pranav Ashar *Using Range Analysis for Software Verification*, 4th International Workshop on Software Verification and Validation (SVV), Seattle, USA, 2006.
16. C. Wang, Z. Yang, F. Ivancic, and A. Gupta, *Disjunctive Image Computation for Embedded Software Verification*, Design, Automation and Test in Europe (DATE), Munich, Germany. March 2006.
17. Y. Lu, S. Lu, F. Fotouhi, Z. Yang and Y. Sun, *PDC: Pattern Discovery with Confidence in DNA Sequences*, IASTED International Conference on Advances in Computer Science and Technology, Puerto Vallarta, Mexico, 2006.
18. F. Ivancic, I. Shlyakhter, A. Gupta, M. K. Ganai, V. Kahlon, C. Wang, and Z. Yang, *Model Checking C Programs Using F-Soft*, invited paper, IEEE International Conference on Computer Design (ICCD), 2005.
19. F.Ivancic, Z. Yang, M. Ganai, A. Gupta, I. Shlyakhter and P.Ashar, *F-Soft: Software Verification Platform*, 17th International Conference on Computer-Aided Verification (CAV), 2005.
20. V. Bhuse, A. Gupta, M. Terwilliger, Z. Kamal, and Z. Yang, *Using Routing Data for Information Authentication in Sensor Networks*, 3rd International Trusted Internet Workshop, 2004.
21. F.Ivancic, Z. Yang, M. Ganai, A. Gupta, and P.Ashar, *Efficient SAT-based Bounded Model Checking for Software Verification*, 1st International Symposium on Leveraging Applications of Formal Methods (ISoLA), 2004.
22. Z. Yang and R.Alur, *Variable Reuse for Efficient Image Computation*, 5th International Conference on Formal Methods in Computer-Aided Design (FMCAD), 2004.
23. W.Shen, Z. Yang and M.Guizani, *Execution of a Requirement Model in Software Development*, ISCA 13th International Conference on Intelligent & Adaptive Systems and Software Engineering (IASSE), 2004.

24. A. Gupta, M. Ganai, Z. Yang and P. Ashar, *Iterative Abstraction using SAT-based BMC with Resolution*, International Conference on Computer Aided Design(ICCAD), 2003.
25. A. Gupta, M. Ganai, C. Wang, Z. Yang and P. Ashar, *Abstraction and BDDs Complement SAT-Based BMC in DiVer*, 15th International Conference on Computer-Aided Verification(CAV), 2003.
26. M. Ganai, A. Gupta, Z. Yang and P. Ashar, *Efficient Distributed SAT and SAT-based Distributed Bounded Model Checking*, 12th Advanced Research Working Conference on Correct Hardware Design and Verification Methods(CHARME), 2003.
27. A. Gupta, C. Wang, M. Ganai, Z. Yang, and P. Ashar, *Learning from BDDs in SAT-based Bounded Model Checking*, 40th Design Automation Conference(DAC), 2003.
28. R. Alur, M. McDougall, and Z. Yang, *Exploiting Behavioral Hierarchy for Efficient Model Checking*, 14th International Conference on Computer-Aided Verification(CAV), 2002.
29. A. Gupta, Z. Yang, P. Ashar, L. Zhang and S. Malik, *Partition-Based Decision Heuristics for Image Computation Using SAT and BDDs*, International Conference on Computer Aided Design(ICCAD), 2001.
30. A. Gupta, A. Gupta, Z. Yang, and P. Ashar, *Dynamic Detection and Removal of Inactive Clauses in SAT with Application in Image Computation*, 38th Design Automation Conference(DAC), 2001.
31. K. Fisler, R. Fraer, G. Kamhi, M. Vardi, and Z. Yang, *Is There a Best Symbolic Cycle-Detection Algorithm?* Tools and Algorithms for the Construction and Analysis of Systems (TACAS), 2001.
32. A. Gupta, Z. Yang, A. Gupta and P. Ashar, *SAT Based State Reachability Analysis and Model Checking*, 3rd International Conference on Formal Methods in Computer-Aided Design (FMCAD), 2000.

#### **United States Patents**

1. A. Gupta, Z. Yang and P. Ashar, *SAT-Based Image Computation with Application in Reachability Analysis*, Patent Number: 6,728,665, April 27, 2004.
2. A. Gupta, A. Gupta, Z. Yang and P. Ashar, *Dynamic Detection and Removal of Inactive Clauses in SAT with Application in Image Computation*, Patent Number: 6,496,961, December 17, 2002.
3. A. Gupta, Z. Yang, P. Ashar and S. Malik, *Partition-based decision heuristics for SAT and image computation using SAT and BDDs*, Patent Number: 6,651,234, November 18, 2003.
4. A. Gupta, M. Ganai, Z. Yang, and P. Ashar, *Efficient distributed SAT and SAT-based distributed bounded model checking*, Patent Number: 7,203,917, April 10, 2007.
5. F. Ivancic, Z. Yang, A. Gupta, M. Ganai, and P. Ashar, *System and Method for Modeling, Abstraction, and Analysis of Software*, Patent Number: 7,346,486, March 18, 2008.
6. C. Wang, Z. Yang, and A. Gupta, *Reachability Analysis for Program Verification*, Published United States Patent Application 20080016497, January 17, 2008.
7. C. Wang, A. Gupta, Z. Yang, and F. Ivancic, *Disjunctive image computation for sequential systems*, Published United States Patent Application 20070044084, February 22, 2007.
8. S. Cadambi, A. Zaks, F. Ivancic, I. Shlyakhter, Z. Yang, M. Ganai, A. Gupta, and P. Ashar, *Software Verification Using Range Analysis*, Published United States Patent Application 20060282806, December 14, 2006.
9. A. Gupta, M. Ganai, Z. Yang, and P. Ashar, *Iterative abstraction using SAT-based BMC with proof analysis*, Published United States Patent Application 20040230407, November 18, 2004.

10. M. Ganai, L. Zhang, A. Gupta, Z. Yang, and P. Ashar, *Efficient approaches for bounded model checking*, Published United States Patent Application 20030225552, December 4, 2003.

**Book Chapter**

1. Z.H. Kamal, L. Lilien, A. Gupta, Z. Yang, M. Batsa, *A New UMA Paradigm: Class 2 Opportunistic Networks*, book chapter in: Y. Zhang, L.T. Yang, J. Ma (Eds.), *Unlicensed Mobile Access Technology: Protocols, Architectures, Security, Standards and Applications*, Auerbach Publications, Taylor&Francis Group, Boca Raton, FL (to appear).

PROFESSIONAL  
AWARDS AND  
RECOGNITION

- ACM TODAES Best Paper Award, 2008.
- IEEE senior member since July 2008.
- Outstanding New Researcher Award, College of Engineering and Applied Sciences, Western Michigan University, 2008.